AMENTMENTS

Amendments to the claim

1-60. (canceled)

61. (currently amended) A chip packaging method comprising:

providing a bulk metal substrate without conductive traces~~with a surface~~;

providing a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface~~, whereas the backside of each die is adhered to the surface of the metal substrate~~;

mounting the dies onto the bulk metal substrate, the backside of the dies facing the bulk metal substrate; and

~~allocating a first dielectric layer on top of the surface of the metal substrate and the active surface of the dies;~~

forming~~allocating~~ a plurality of patterned lines ~~first patterned wiring layer~~ over the active surface of the dies, wherein the patterned lines are constructed from at least a patterned wiring layer.~~on top of the first dielectric layer, wherein the first patterned wiring layer is electrically connected to the metal pads of the dies through the first dielectric layer, extends to a region outside of an area above the active surfaces of the dies, and has a plurality of first bonding pads.~~

62. (original) The method of claim 61, wherein the dies perform same functions.

63. (original) The method of claim 61, wherein the dies perform different functions.

64. (currently amended) The method of claim 61, wherein the bulk metal substrate has a plurality of cavities ~~inwardly protruded areas~~ located on the surface of the bulk metal substrate, where the backside of each die is adhered to a bottom of the cavities ~~an inwardly protruded area~~.

65. (currently amended) The method of claim 64, wherein a depth of the cavities ~~inwardly protruded areas~~ is equal to a thickness of the dies.

66. (currently amended) The method of claim 64, wherein the cavities ~~inwardly protruded areas~~ are formed by machining.

67. (currently amended) The method of claim 61, wherein the bulk metal substrate comprises ~~comprising~~ a first metal layer and a second metal layer, the first metal layer is mounted on the second layer, ~~formed overlapping, a surface of the metal substrate is a side of the second metal layer that is further away from the first metal layer,~~ the first metal layer has a plurality of~~at least one~~ openings that penetrates through the first metal layer and expose the second metal layer ~~used~~ to form a plurality of cavities~~an inwardly protruded areas~~, ~~and~~ the backside of the dies is mounted on the second metal layer, and the patterned lines formed over the second metal layer ~~adhered to a bottom of the inwardly protruded areas~~.

68. (original) The method of claim 67, wherein a thickness of the first metal layer is approximately equal to a thickness of the dies.

69. (currently amended) The method of claim 67, wherein the steps ~~a method~~ of forming the metal layer comprise: ~~openings on the first metal layer comprising~~

punching ~~and then overlapping~~ the first metal layer to form the openings that penetrate through the first metal layer; and

overlapping the first metal layer and the second metal layer ~~to form the metal substrate~~.

70. (currently amended) The method of claim 61, ~~wherein after adhering the dies and before allocating the first dielectric layer,~~ further comprising forming ~~allocating~~ a filling layer over ~~on top of the surface of~~ the bulk metal substrate and surrounding the peripheral region of the

dies after mounting the dies onto the bulk metal substrate, ~~and~~ wherein a top surface of the filling layer is planar to the active surface of the dies and the patterned lines are formed over the filling layer.

71. (original) The method of claim 70, wherein a material of the filling layer is selected from a group consisting of epoxy and polymer.

72. (currently amended) The method of claim 61, further comprising forming a dielectric layer over the active surface of the dies after mounting the dies onto the bulk metal substrate and before forming the patterned lines over the active surface of the dies. ~~wherein after allocating the first dielectric layer and before allocating the first patterned wiring layer, further comprising patterning the first dielectric layer to form a plurality of first thru holes that penetrates through the first dielectric layer, and the first patterned conductive is electrically connected to the metal pads of the dies by the first thru holes.~~

73. (currently amended) The method of claim 72, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material. ~~wherein when allocating the first patterned wiring layer on the first dielectric layer, further includes allocating a plurality of first vias by filling part of a conductive material of the first patterned conductive layer into the thru holes to electrically connect the first patterned wiring layer and the metal pads of the dies by the first vias.~~

74. (currently amended) The method of claim 61~~72~~, further comprising forming a dielectric layer over the patterned lines after forming the patterned lines over the active surface of the dies. ~~wherein when allocating the first patterned wiring layer on top of the first dielectric layer, further comprising filling the first thru holes with a conductive material to form a plurality~~

~~of first vias, by which the first patterned wiring layer and the metal pads are electrically connected.~~

75. (currently amended) The method of claim 7461, wherein a material of the ~~first~~ dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

76. (currently amended) The method of claim 61, wherein the step of forming the patterned lines over the active surface of the dies is provided by a technology comprising ~~method of allocating the first patterned wiring layer on top of the first dielectric layer is selected from a group consisting of sputtering,~~ electroplating~~., and electro-less plating.~~

77. (currently amended) The method of claim 61, wherein the step of forming the patterned lines over the active surface of the dies is provided by a technology comprising sputtering and electroplating.~~further comprising allocating a patterned passivation layer on top of the first dielectric layer and the first patterned wiring layer and exposing the first bonding pads.~~

78. (currently amended) The method of claim 61, further comprising ~~allocating~~ depositing a plurality of ~~a~~ bonding points on a plurality of ~~the first~~ bonding pads of the patterned lines after forming the patterned lines over the active surface of the dies.

79. (currently amended) The method of claim 78, wherein the bonding points comprise ~~are selected from a group consisting of~~ solder balls~~., bumps, and pins.~~

80. (currently amended) The method of claim 6178, further comprising performing a singularizing process to form a plurality of chip package structures ~~singularizing the chip package structure~~ after forming the patterned lines over the active surface of the dies. ~~allocating the bonding point on the bonding pads.~~

81. (currently amended) The method of claim 80, wherein each chip package structure has ~~a singularization of the chip package structure is performed on~~ a single die.

82. (currently amended) The method of claim 80, wherein each chip package structure has ~~a singularization of the chip package structure is performed on~~ a plurality of dies.

83. (currently amended) The method of claim 61, wherein the step of forming the patterned lines over the active surface of the dies comprises forming a single patterned wiring layer.~~further comprising:~~

~~(a) allocating a second dielectric layer on top of the first dielectric layer and the first patterned wiring layer; and~~

~~(b) allocating a second patterned wiring layer on top the second dielectric layer, wherein the second patterned wiring layer is electrically connected to the first patterned wiring layer through the second dielectric layer, and the second patterned wiring layer extends to a region outside the active surface of the die and has a plurality of second bonding pads.~~

84. (currently amended) The method of claim 61~~83~~, wherein the step of forming the patterned lines over the active surface of the dies comprises forming a plurality of patterned wiring layers and at least a dielectric layer, the dielectric layer formed between the patterned wiring layers. ~~wherein after allocating the second dielectric layer and before allocating the second patterned wiring layer, further comprising patterning the second dielectric layer to form a plurality of second thru holes, which corresponds to the first thru holes and penetrates the second dielectric layer, to electrically connect to the first patterned wiring layer.~~

85. (currently amended) The method of claim 84, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric

material, and stress buffer material. ~~wherein when allocating the second patterned wiring layer on top of the second dielectric layer, further comprising filling the second thru-holes with part of a conductive material of the second patterned wiring layer to form a plurality of second vias, by which the second patterned wiring layer is electrically connected to the first patterned wiring layer.~~

86. (currently amended) The method of claim 6184, wherein the step of forming the patterned lines over the active surface of the dies comprises forming a passive device over the active surface of the dies. ~~before allocating the second patterned wiring layer on top of the second dielectric layer, further comprising filling the second thru-holes with a conductive material to form a plurality of second vias, by which the second patterned wiring layer is electrically connected to the first patterned wiring layer.~~

87. (currently amended) The method of claim 8683, wherein the passive device comprises a capacitor. ~~a material of the second dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.~~

88. (currently amended) The method of claim 8683, wherein the passive device comprises a resistor. ~~the method of allocating the second patterned wiring layer on the second dielectric layer is selected from a group consisting of sputtering, electroplating, and electro-less plating.~~

89. (currently amended) The method of claim 8683, wherein the passive device comprises an inductor. ~~further comprising allocating a patterned passivation layer on top of the second dielectric layer and the second patterned wiring layer and exposing the second bonding pads.~~

90. (currently amended) The method of claim 8683, wherein the passive device comprises a wave-guide. ~~further comprising allocating a bonding point on the second bonding pads.~~

91. (currently amended) The method of claim 8690, wherein the passive device comprises a filter. ~~wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.~~

92. (currently amended) The method of claim 8690, wherein the passive device comprises a micro electronic mechanical sensor (MEMS). ~~further comprising singularizing the chip package structure after allocating the bonding point on the second bonding pads.~~

93. (currently amended) The method of claim 6192, wherein the bulk metal substrate is constructed from copper. ~~a singularization of the chip package structure is performed on a single die.~~

94. (currently amended) The method of claim 6192, wherein the bulk metal substrate is constructed from aluminum alloy. ~~a singularization of the chip package structure is performed on a plurality of dies.~~

95-101. (canceled)

102. (currently amended) A chip packaging method comprising:

providing a first substrate ~~with a first surface~~;

providing a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, ~~whereas the active surface of each die is adhered to the first surface of the substrate~~;

mounting the dies over the first substrate, the active surfaces of the dies facing the first substrate;

~~allocating a first filling layer on top of the first surface of the substrate and surrounding the dies;~~

~~planarizing and~~ thinning ~~of the first filling layer and~~ the dies from their backsides;

providing a second ~~metal~~ substrate~~; with a second surface and adhering the second surface of the metal substrate to the first filling layer and the dies;~~

mounting the second substrate over the backsides of the dies;

removing the first ~~first filling layer and the~~ substrate; and

~~allocating a first dielectric layer on the second surface of the metal substrate and the active surface of the dies; and~~

forming a plurality of patterned lines over the active surface of the dies ~~allocating a first patterned wiring layer on top of the first dielectric layer, wherein the first patterned wiring layer is electrically connected to the metal pads of the dies through the first dielectric layer, extends to a region outside the active surfaces of the dies, and has a plurality of first bonding pads.~~

103. (original) The method of claim 102, wherein the dies perform same functions.

104. (original) The method of claim 102, wherein the dies perform different functions.

105. (currently amended) The method of claim 102, wherein a material of the first substrate is selected from a group consisting of glass, silicon, and organic material.

106. (currently amended) The method of claim 102, further comprising forming a filling layer over the first substrate and surrounding the dies ~~wherein~~ before thinning the dies from their backsides.~~a material of the first filling layer is selected from a group consisting of epoxy and polymer.~~

107. (currently amended) The method of claim 10~~6~~2, wherein the step of thinning the dies from their backsides comprises thinning the filling layer and the dies using a chemical mechanical polishing (CMP) process. ~~after adhering the metal substrate and before removing the~~

~~first filling layer and the substrate, further comprising allocating a second filling layer on top of the second surface of the metal substrate, the second filling layer surrounds a peripheral of the dies and has a top surface that is planar to the active surface of the dies.~~

108. (currently amended) The method of claim 106~~7~~, wherein a material of the ~~second~~ filling layer is selected from a group consisting of epoxy and polymer.

109. (currently amended) The method of claim 102, further comprising forming a filling layer over the second substrate and surrounding the dies after mounting the second substrate over the backsides of the dies, wherein a top surface of the filling layer is planar to the active surface of the dies and the patterned lines are formed over the filling layer.~~wherein after allocating the first dielectric layer and before allocating the first patterned wiring layer, further comprising patterning the first dielectric layer to form a plurality of first thru holes, by which the first patterned wiring layer is electrically connected to the metal pads of the dies.~~

110. (currently amended) The method of claim 109, wherein a material of the filling layer is selected from a group consisting of epoxy and polymer. ~~when allocating the first patterned wiring layer on top of the first dielectric layer, further comprising filling the first thru holes with part of a conductive material of the first patterned wiring layer to form a plurality of first vias, by which the first patterned wiring layer is electrically connected to the metal pads of the dies.~~

111. (currently amended) The method of claim 109, further comprising forming a dielectric layer over the active surface of the dies after mounting the dies onto the second substrate and before forming the patterned lines over the active surface of the dies.~~wherein before allocating the first patterned wiring layer on top of the first dielectric layer, further comprising~~

~~filling the first thru-holes with a conductive material to form a plurality of first vias, by which the first patterned wiring layer is electrically connected to the metal pads of the dies.~~

112. (currently amended) The method of claim 1110~~2~~, wherein a material of the ~~first~~ dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

113. (currently amended) The method of claim 102, wherein the step of forming the patterned lines over the active surface of the dies is provided by a technology comprising ~~a method of allocating the first patterned wiring layer on the first dielectric layer is selected from a group consisting of sputtering,~~ electroplating. ~~, and electro-less plating.~~

114. (currently amended) The method of claim 102, wherein the step of forming the patterned lines over the active surface of the dies is provided by a technology comprising sputtering and electroplating. ~~further comprising allocating a patterned passivation layer on top of the first dielectric layer and the first patterned wiring layer and exposing the first bonding pads.~~

115. (currently amended) The method of claim 102, further comprising depositing a plurality of bonding points on a plurality of bonding pads of the patterned lines after forming the patterned lines over the active surface of the dies. ~~allocating a bonding point on the first bonding pads.~~

116. (currently amended) The method of claim 115, wherein the bonding points comprise ~~are selected from a group consisting of~~ solder balls. ~~, bumps, and pins.~~

117. (currently amended) The method of claim 102~~15~~, further comprising performing a singularizing process to form a plurality of chip package structures after forming the patterned

lines over the active surface of the dies.~~singularizing the chip package structure after allocating the bonding point on the first bonding pads.~~

118. (currently amended) The method of claim 117, wherein each chip package structure has ~~a singularization of the chip package structure is performed on~~ a single die.

119. (currently amended) The method of claim 117, wherein each chip package structure has ~~a singularization of the chip package structure is performed on~~ a plurality of dies.

120. (currently amended) The method of claim 102, wherein the step of forming the patterned lines over the active surface of the dies comprises forming a single patterned wiring layer. ~~further comprising:~~

~~(a) allocating a second dielectric layer on top of the first dielectric layer and the first patterned wiring layer; and~~

~~(b) allocating a second patterned wiring layer on top the second dielectric layer, wherein the second patterned wiring layer is electrically connected to the first patterned wiring layer through the second dielectric layer, and the second patterned wiring layer extends to a region outside the active surface of the die and has a plurality of second bonding pads.~~

121. (currently amended) The method of claim 102~~120~~, wherein the step of forming the patterned lines over the active surface of the dies comprises forming a plurality of patterned wiring layers and at least a dielectric layer, the dielectric layer formed between the patterned wiring layers.~~after allocating the second dielectric layer and before allocating the second patterned wiring layer, further comprising patterning the second dielectric layer to form a plurality of second thru holes, which corresponds to the first bonding pads and penetrates the second dielectric layer, to electrically connect to the first patterned wiring layer.~~

122. (currently amended) The method of claim 121, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material. ~~when allocating the second patterned wiring layer on top of the second dielectric layer, further comprising filling the second thru-holes with part of a conductive material of the second patterned wiring layer to form a plurality of second vias, by which the second patterned wiring layer is electrically connected to the first patterned wiring layer.~~

123. (currently amended) The method of claim 102~~121~~, further comprising forming a dielectric layer over the patterned lines after forming the patterned lines over the active surface of the dies. ~~wherein before allocating the second patterned wiring layer on top of the second dielectric layer, further comprising filling the second thru-holes with a conductive material to form a plurality of second vias, by which the second patterned wiring layer is electrically connected to the first patterned wiring layer.~~

124. (currently amended) The method of claim 123~~120~~, wherein a material of the ~~second~~ dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

125. (currently amended) The method of claim 102~~120~~, wherein the step of forming the patterned lines over the active surface of the dies comprises forming a passive device over the active surface of the dies. ~~a method of allocating the second patterned wiring layer on the second dielectric layer is selected from a group consisting of sputtering, electroplating, and electro-less plating.~~

126. (currently amended) The method of claim 125~~120~~, wherein the passive device comprises a capacitor.~~further comprising allocating a patterned passivation layer on top of the second dielectric layer and the second patterned wiring layer and exposing the second bonding pads.~~

127. (currently amended) The method of claim 125~~120~~, wherein the passive device comprises a resistor.~~further comprising allocating a bonding point on the second bonding pads.~~

128. (currently amended) The method of claim 125~~127~~, wherein the passive device comprises an inductor.~~wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.~~

129. (currently amended) The method of claim 125~~127~~, wherein the passive device comprises a wave-guide.~~further comprising singularizing the chip package structure after allocating the bonding point on the second bonding pads.~~

130. (currently amended) The method of claim 125~~129~~, wherein the passive device comprises a filter.~~wherein a singularization of the chip package structure is performed on a single die.~~

131. (currently amended) The method of claim 125~~129~~, wherein the passive device comprises a micro electronic mechanical sensor (MEMS).~~a singularization of the chip package structure is performed on a plurality of dies.~~

132. (currently amended) The method of claim 102~~120~~, wherein the second substrate is constructed from a pure metal or metal alloy. ~~further comprising repeating step (a) and step (b) a plurality of times.~~

133. (currently amended) The method of claim 102~~132~~, wherein the second substrate is constructed from copper.~~further comprising allocating a patterned passivation layer on the second dielectric layer and the second patterned wiring layer that are furthest away from the metal substrate and exposing the second bonding pads of the second patterned wiring layer that is furthest away from the metal substrate.~~

134. (currently amended) The method of claim 132, wherein the second substrate is constructed from aluminum alloy.~~further comprising allocating a bonding point on the second bonding pads of the second patterned wiring layer that is furthest away from the metal substrate.~~

135-138. (canceled)